CLAIMS 09/575,560

Sub B1

1. A system comprising:

a DAC that receives a multi-bit digital signal and outputs at least two analog signals each indicative of a sum of values of bits in the multi-bit digital signal.

2. The system of claim 1 wherein the at least two analog signals are substantially equal to each other.

3 The system of claim 1 wherein the DAC comprises a switched capacitor DAC.

Sub B2

4. A method comprising:

receiving a multi-bit digital signal ; and

generating at least two analog output signals each indicative of a sum of values of bits in the multi-bit digital signal.

5. The method of claim 4 wherein generating comprises generating at least analog output signals that are substantially equal to one another.

6. The method of claim 5 wherein generating comprises:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal; and

connecting at least two of the plurality of capacitors to one another to share charge with one another.

Sub B3

7. A system comprising:

means for receiving a multi-bit digital signal ; and

means for generating at least two analog output signals each indicative of a sum of values of bits in the multi-bit digital signal.

8. The system of claim 7 wherein the means for generating comprises means for generating at least two analog output signals that are substantially equal to one another.

9. The system of claim7 wherein means for generating comprises a switched capacitor DAC.

10. A switched capacitor filter having a first switched capacitor comprising a switched capacitor without substantial effects from parasitic characteristics, and a second switched capacitor in parallel with the first switched capacitor, the second switched capacitor having effects from parasitic characteristics.

11. A system comprising,

a switched capacitor filter having a first switched capacitor comprising a switched capacitor and a second switched capacitor in parallel with the first switched capacitor, the second switched capacitor having characteristics including parasitic effects;

a DAC having a switched capacitor having characteristics including parasitic effects substantially corresponding to the parasitic effects of the second switched capacitor of the switched capacitor filter.

12. An apparatus comprising:

A first switched capacitor cell having a reference direction and being adapted to electrically connect to a second switched capacitor cell substantially identical to the first switched capacitor cell, the second switched capacitor cell having a reference direction and being oriented such that the reference direction of the second switched capacitor cell is directed in substantially the same direction as the reference direction of the first switched capacitor cell, and being adapted to electrically connect to a third switched capacitor cell substantially identical to the first switched capacitor cell, the third switched capacitor cell having a reference direction and being oriented such that the reference direction of the third switched capacitor cell is directed in direction angularly offset from the direction in which the reference direction of the first switched capacitor cell is directed.

13. The apparatus of claim 12 wherein the second switched capacitor cell and the third switched capacitor cell are adjacent to the first switched capacitor cell.

14. The apparatus of claim 13 wherein the first, second, and third switched capacitor cells are rectangular.

15. The apparatus of claim 13 wherein the first, second, and third switched capacitor cells are substantially square.

15. The apparatus of claim 13 wherein the angular offset is substantially ninety degrees.

16. A system comprising:

a binary weighted DAC; and

a segmented DAC, coupled to the binary weighted DAC, the segment DAC comprising a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, at least two of the plurality of sub DACs sharing charge with one another, and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

17. A system comprising:

a scrambler that receives input and provides output; and

and a switched capacitor DAC that has a plurality of capacitors and redistributes charge between at least two of the plurality of capacitors, coupled to the scrambler, that receives digital output of the scrambler.

18. A system as claimed in claim 17 wherein the scrambler comprises a plurality of outputs, the DAC comprises a plurality of inputs greater than the number of outputs of the scrambler.

19. The system of claim 18 wherein at least one of the inputs to the scrambler is coupled to a first logic signal, and at least one of the inputs to the DAC is coupled to a second logic signal having a logic state opposite a logic state of the first signal.

20. The system of claim 19 wherein there is a predetermined relationship between the first logic signal and the second logic signal.

21. The system of claim 19 wherein the first logic signal and the second logic signal do not change logic state .

22. A digital to analog converter that receives a multi-bit digital signal and produces an analog output that is proportional to the square of the multi-bit digital signal.

23. The digital to analog convert of claim 22 wherein the multi-bit digital signal is an equally-weighted multi-bit input signal.

24. The digital to analog convert of claim 22 wherein the multi-bit digital signal is a binarily- weighted multi-bit input signal.

25. An analog to digital converter having an analog comparison stage coupled to a digital latch stage, the analog to digital converter comprising:

a feedback element through which an output of the digital latch stage is coupled back to an input of the analog comparison stage, wherein the feedback element comprises a digital to analog converter according to claim 21.

26. A method for use in an analog to digital converter having an analog comparison stage coupled to a digital latch stage the method comprising:

coupling an output of the digital latch stage back to an input of the analog comparison stage through a digital to analog converter that receives a multi-bit digital signal and produces an analog output proportional to the square of the multi-bit digital signal.

27. A handset for a mobile communication system comprising:

an input stage that receives an input signal and outputs a multi-bit digital signal to a digital-to-analog conversion system that receives the multi-bit digital signal and outputs an analog signal indicative of a sum of values of bits in the multi-bit signal, and comprising:

a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the

multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associate bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, at least two of the plurality of sub DACs sharing charge with one another, and the switched capacitor network outputs at least one analog signal indicative of a sum of values of bits in the multi-bit signal.

28. A system comprising a digital signal processing stage that receives input and provides output; and a switched capacitor DAC that has a plurality of capacitors and redistributes charge between at least two of the plurality of capacitors, coupled to the digital signal processing stage, that receives digital output of the digital signal processing stage.

29. A digital to analog converter receives a first multi-bit digital signal and a second multi-bit digital signal ,and produces an analog output that is indicative a product of the first multi-bit digital signal and the second multi-bit digital signal.

30. An analog to digital converter having an analog comparison stage coupled to a digital latch stage, a feedback element through which an output of the digital latch stage is coupled back to an input of the analog comparison stage, the analog to digital converter comprising:

a feedback element that includes a digital to analog converter that receives a first multi-bit digital signal and a second multi-bit digital signal ,and produces an analog output that is indicative a product of the first multi-bit digital signal and the second multi-bit digital signal.